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# SUBSTITUTE SPECIFICATION

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# DESCRIPTION

# INVERTER DEVICE

## TECHNICAL FIELD

[0001] The present invention relates to an inverter device. More~~, more~~ specifically, the present invention relates to an inverter device including a ~~circuit for preventing compression destruction and malfunction of a~~ high-withstand-voltage ~~compression integrated circuit (~~IC~~)~~ that performs drive control on a switching element of an inverter circuit~~ provided with a switching element for driving load~~.

## BACKGROUND ART

[0002] In a typical~~conventional~~ inverter device, a switching element is used to drive ~~as a countermeasure for~~ a load. Moreover, a high-withstand-voltage IC is used to drive control the switching of the switching element. A negative surge, however, is generated when the switching element performs switching. The negative surge~~ that~~ is generated due to a variation in ~~an amount of change of~~ current ~~(di/dt)~~ per unit time (di/dt) and inductance of the wiring. Patent Document 1 discloses~~ when a switching element that drives load switches,~~ a technology for suppressing the generation of the negative surge. Specifically, Patent Document 1 teaches to connect~~connecting~~ a clamp diode between a low-voltage ~~pressure side~~ reference terminal and a high-voltage~~ pressure side~~ reference terminal of the high-withstand-voltage IC.

[0003] A negative voltage generated due to a small inductance resulting from a chip pattern, wiring, and the like, is the prime cause of the breakdown of the high-withstand-voltage IC. In the technology disclosed in Patent Document 1, the negative voltage is clamped by using the clamp diode to prevent the breakdown of the high-withstand-voltage IC.

[0004] On the other hand, Patent Document 2 teaches to provide a voltage divider circuit (resistance element) in series with the clamp diode in the configuration disclosed in Patent Document 1.

[0005] Not all the negative voltage, however, can be suppressed with the clamp diode. ~~a high compression IC that performs drive control of the switching element is disclosed~~

~~(refer to Patent Document 1).~~

~~[0003] The technology disclosed in Patent Document 1 prevents destruction of the high compression IC by clamping, with the clamp diode, a negative voltage that occurs due to a slight inductance such as a chip pattern or wiring that causes destruction of the high compression IC.~~

~~[0004] In addition to the clamp diode disclosed in Patent Document 1, an example of a configuration of an inverter device provided with a voltage dividing circuit (resistance element) connected in series with the clamp diode is disclosed (refer to Patent Document 2).~~

~~[0005]~~ In the technology disclosed in Patent Document 2, ~~negative voltage applied to the high compression IC is reduced by dividing~~ the negative voltage, which cannot be suppressed with~~only by~~ the clamp diode, is divided by using~~with~~ the clamp diode and the resistance element of the voltage divider~~dividing~~ circuit to reduce the level of the negative voltage applied to the high-withstand-voltage IC.~~,~~

[0006] [Patent Document 1] Japanese Patent Application Laid-open~~-Open~~ No. H10-42575

[Patent Document 2] Japanese Patent No. 3577478

DISCLOSURE OF INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION

[0007] However, in the ~~conventional~~ technology disclosed in Patent Document 1, there is a possibility that the circulating current flows through the clamp diode itself. As a result, ~~and~~ a diode ~~connected back-to-back to the switching element~~ of a larger current rating (a diode of substantially the same rating as the reverse-~~lower arm (diode for flowing circulating current) are connected in~~ parallel connected diode) needs to be used. This is disadvantageous, because diodes of larger current rating are relatively costlier and bigger.~~, and therefore, there is a possibility that the circulating current will flow in the clamp diode itself. Accordingly, a diode of a large current rating needs to be employed (a diode of a substantially same rating as the back-to-back connected diode), which directly leads to increases in cost and size.~~

[0008] On the other hand, in the ~~conventional~~ technology disclosed in Patent Document 2, there is a possibility that a circulating current flows through ~~will flow into~~ both the

clamp diode and the voltage divider~~dividing~~ circuit. As~~Accordingly, similarly to the conventional technology disclosed in Patent Document 1, both~~ a result, ~~diode of~~ a larger current rating ~~diode~~ and a larger current rating resistance element need to be used. This is disadvantageous, because diodes of larger current rating are relatively costlier~~employed,~~ and bigger. Moreover, larger current rating resistance elements are relatively costlyier~~therefore, the disadvantage of increases in cost~~ and bigger.~~size cannot be avoided.~~

[0009] A typical high-withstand-voltage~~compression~~ IC includes, for example, an input buffer, an ~~a metal-oxide (~~MOS~~)~~ transistor, a resistor, a driver circuit, and the like. Therefore, if~~so forth. Thus, when~~ a negative voltage described as above is generated, sometimes a through current flows through parasitic capacitance~~capacity~~ of the MOS transistor into the high-withstand-voltage~~compression~~ IC thereby generating a~~. A latch up~~ phenomenon called as latch-up. The latch-up phenomenon is a phenomenon~~,~~ in which the driver circuit of~~in~~ the high-withstand-voltage~~compression~~ IC outputs an erroneous signal due to the presence of~~, is caused by~~ the through current. The conventional technologies disclosed in Patent Documents 1 and 2 have been ~~are~~ insufficient for suppressing~~solving~~ the generation~~problem~~ of the latch--up phenomenon.~~.~~

[0010] It is~~The present invention has been made in view of the above, and~~ an object of the present invention ~~is~~ to provide a technology ~~an inverter device~~ that can prevent breakdown~~destruction~~ and malfunction (latch--up phenomenon) of a high-withstand-voltage~~compression~~ IC in~~for controlling~~ an inverter device without much increasing the~~circuit, and providing circuit technology that can suppress increases in~~ circuit scale or~~and~~ cost.

MEANS FOR SOLVING PROBLEM

[0011] To solve the above problems and to achieve the above objects, an inverter device according to an aspect of the present invention includes an inverter circuit that includes a ~~including a~~ bridge circuit connected between a positive electrode and a negative electrode of a direct--current power supply, the bridge circuit including an upper arm unit including an upper-arm switching element and an upper arm diode ~~and a lower arm unit~~ connected in reverse-parallel ~~series, wherein the upper arm unit includes a upper arm switching element and a diode connected back~~-to-~~back to~~ each other;~~,~~ and a lower

arm unit including a ~~the~~ lower~~- arm unit includes a lower~~ arm switching element and a lower arm diode connected in reverse-parallel~~back to back~~ to each other, the lower arm unit being series connected with the upper arm unit; an inverter driving unit including a high-withstand-voltage~~-compression~~ IC that drives switching elements in the upper arm unit ~~the upper arm switching element~~ and the lower~~-arm switching element; and a clamp unit that clamps a difference in potential between a lower~~-arm unit, the high-withstand-voltage IC having a first terminal for supplying a~~driving~~ reference voltage to the switching element in the lower arm unit and a second terminal for supplying a~~supply terminal of the high compression IC and an upper arm driving~~ high-voltage to the switching element in the the upper arm unit; and a clamp unit that clamps a potential difference between the first terminal and the second terminal.~~pressure side power supply terminal of the high compression IC.~~

[0012] According to the present invention, the clamp unit clamps a potential ~~above aspect, a clamping means for clamping a~~ difference ~~in potential~~ between the first~~a lower arm driving reference supply~~ terminal ~~of a high compression IC~~ and the second terminal of the high-withstand-voltage IC. In other words, the clamp unit clamps the ~~an upper arm driving high-pressure side power supply terminal of the high compression IC clamps a~~ negative voltage that causes voltage breakdown of the high-withstand-voltage~~compression destruction in the high compression~~ IC due to wiring inductance and circulating current, whereby the~~and reduces~~ through current that is to flow into the high-withstand-voltage IC is reduced~~flowing inside the high compression IC~~.

EFFECT OF THE INVENTION

[0013] According to the~~an~~ inverter device of the present invention, the ~~a~~ clamping unit clamps the potential ~~means for clamping a~~ difference ~~in potential~~ between the~~a lower arm driving~~ reference power-supply terminal of the~~a~~ high-withstand-voltage ~~compression~~ IC and the~~an upper arm driving~~ high-voltage~~pressure side~~ power-supply terminal of the high-withstand-voltage~~-compression~~ IC. In other words, the clamp unit clamps a negative voltage that causes the voltage breakdown of~~compression destruction in~~ the high-withstand-voltage~~-compression~~ IC, whereby~~and prevents~~ a large portion of the through current is prevented from flowing into~~inside~~ the high-withstand-voltage ~~compression~~ IC. Therefore, the inverter device can prevent occurrence of

breakdown~~destruction~~ and malfunction (latch--up phenomenon) of the high-withstand-voltage ~~-compression~~ IC ~~can be prevented~~, and suppresses increases in circuit scale and cost ~~can be suppressed~~.

BRIEF DESCRIPTION OF DRAWINGS

[0014] Fig. 1 is a schematic diagram for explaining an inverter device (single-phase inverter configuration) according to a first embodiment of the present invention.

Fig. 2 is a schematic diagram for explaining~~describing~~ malfunction of a high-withstand-voltage ~~-compression~~ IC in an inverter device that does not include a ~~in which a~~ clamp diode. ~~is not connected.~~

Fig. 3 is a schematic diagram for illustrating~~describing~~ a state in which a through current flowing toward a high-withstand-voltage ~~-compression~~ IC is drawn to a ~~side of a~~ clamp diode in the inverter device according to the first embodiment.

Fig. 4 is a schematic diagram for explaining an inverter device (three-phase inverter configuration: individual~~independent~~ power supply) according to a second embodiment of the present invention.

Fig. 5 is a schematic diagram for explaining an inverter device (three-phase inverter configuration: common power supply) according to a third embodiment of the present invention.

EXPLANATIONS OF SYMBOLS~~LETTERS OR NUMERALS~~

[0015]

2, 2a inverter driving unit

3, 3a inverter circuit

4, 4a, 4b, 4c upper arm unit

5, 5a, 5b, 5c lower arm unit

6, 6a bridge circuit

7 DC power supply

8 load

10, 10a high-withstand-voltage ~~-compression~~ IC

12 driver circuit

14 input buffer

16 NMOS transistor

~~17 parasitic diode~~

20 resistor

C1, C2, C3, C5 decoupling capacitor~~condenser~~

D1, D3, D5 upper--arm diode

D2, D4, D6 lower--arm diode

D10, D11, D12, D13, D21, D22, D23 clamp diode

D17 parasitic diode

R1, R2, R3, R4, R5, R6 gate resistor

T1, T3, T5 upper--arm switching element

T2, T4, T6 lower--arm switching element

## BEST MODE(S) FOR CARRYING OUT THE INVENTION

[0016] Exemplary embodiments of ~~an inverter device according to~~ the present invention will be described below in detail with reference to the accompanying drawings. The present invention is not limited to the ~~these~~ embodiments.

[0017] First Embodiment

Fig. 1 is a schematic diagram for explaining an inverter device according to a first embodiment of the present invention. The inverter device is ~~employs a configuration of~~ a typical single-phase inverter device. In other words, a high-withstand-voltage IC 10 of ~~, in which~~ an inverter driving unit 2 ~~including a high compression IC 10~~ drives both a switching element T1 in an upper arm and a switching element T2 in a lower arm of an inverter circuit 3.

~~[0018]~~ The inverter circuit 3 includes a bridge circuit 6 and a DC power supply 7. The bridge circuit 6 includes a series connected~~device according to the first embodiment is described with reference to Fig. 1.~~

~~[0018] In the inverter circuit 3 shown in Fig. 1, an~~ upper arm unit 4 and lower arm unit 5. The ~~including the switching element (~~upper arm unit 4 includes the switching element (hereinafter, "upper-arm switching element") T1 of ~~in~~ the upper arm and a diode (hereinafter, "upper-~~upper~~ arm diode") D1 connected in reverse-parallel~~back-to-back~~ to each other. The ~~, and a lower arm unit 5 including the switching element (~~lower arm unit 5 includes the switching element (hereinafter, "lower-arm switching element")

T2 of~~in~~ the lower arm and a diode (hereinafter, “lower-~~lower~~ arm diode”) D2 connected in reverse-parallel~~back-to-back~~ to each other. In the~~, are connected in series in a~~ bridge circuit 6, the ~~. A~~ positive electrode of ~~a DC power supply 7 of the bridge circuit 6 is connected to a corrector of~~ the DC power supply 7 is connected to the collector of the upper--arm switching element T1, and the ~~a~~ negative electrode of the DC power supply 7 is connected to the ~~an~~ emitter of the lower-arm switching element T2.

[0019] The high-withstand-voltage IC 10 drives the upper-arm switching element T1 and the lower--arm switching element T2. The high-withstand-voltage IC 10 has various ~~Thus, the inverter circuit 3 shown in Fig. 1 has a configuration of a single-phase inverter circuit.~~

~~[0019] The high compression IC 10 of the inverter driving unit 2 shown in Fig. 1 drives the upper arm switching element T1 and the lower arm switching element T2 in the inverter circuit 3. The high compression IC 10 includes~~ input/output terminals described below. Specifically, the high-withstand-voltage IC 10 has a terminal ~~terminals are a~~ VDD that is a high-voltage~~pressure side~~ power--supply terminal for controlling the high-withstand-voltage ~~compression~~ IC 10, a terminal COM that is a reference power-supply terminal also for controlling the high-withstand-voltage ~~compression~~ IC 10, an upper--arm control--signal input terminal HIN to which a control signal for controlling the upper arm unit 4 is input, a lower--arm control--signal input terminal LIN to which a control signal for controlling the lower arm unit 5 is input, an upper--arm--driving high-voltage~~pressure side~~ power--supply terminal VB connected to a high-voltage ~~pressure side of a~~ driving power--supply that drives the upper arm unit 4, an upper--arm--driving reference power-supply terminal VS that is a reference terminal of the driving power supply that drives the upper arm unit 4, an upper--arm switching-element driving--signal output terminal HO from which a driving signal for driving the upper arm unit 4 is output, a lower--arm--driving high-voltage~~pressure side~~ power-supply terminal VCC that is connected to a high-voltage~~pressure side of a~~ driving power--supply that drives the lower arm unit 5, a lower--arm--driving reference power-supply terminal COM that is a reference terminal of the driving power supply that drives the lower arm unit 5, and a lower--arm switching--element driving--signal output terminal LO from which a driving signal for driving the lower arm unit 5 is output.

[0020] A decoupling capacitor~~condenser~~ C1 is connected between the upper--arm-

driving high-voltage power-supply terminal VB and the upper-arm--driving reference power-~~high-pressure side power supply terminal VB and the upper arm driving reference~~ supply terminal VS. Moreover, a ~~A~~ decoupling capacitor~~condenser~~ C2 is connected between the lower--arm--driving high-voltage~~pressure side~~ power--supply terminal VCC and the lower--arm--driving reference power-supply terminal COM.

[0021] The~~In between the inverter circuit 3 and the high compression IC 10, a gate resistor R1 that controls gate current connects the~~ upper--arm switching--element driving--signal output terminal HO and a gate of the upper--arm switching element T1 are connected through a gate resistor R1 for controlling the gate current, and the~~. The~~ upper--arm--driving reference power-supply terminal VS and an emitter of the upper-arm switching element T1 are connected directly.~~ connected.~~ Similarly, ~~a gate resistor R2 connects~~ the lower--arm switching--element driving--signal output terminal LO and a gate of the lower--arm switching element T2 are connected through a gate resistor R2, and the~~. The~~ lower--arm--driving reference power-supply terminal COM and the emitter of the lower--arm switching element T2 are connected directly.~~ connected.~~

[0022] In the inverter device~~ shown in Fig. 1~~, wiring inductance is minimized as much as possible by taking measures such as ~~, for example,~~ connecting the upper--arm switching element T1 and the lower--arm switching element T2 with a plurality of wires (wire bundle~~bunch~~), directly connecting these switching elements and the output terminals by bonding pads without ~~using~~ wires, and providing a collector~~separating a corrector~~ and an emitter of each switching element separately onto the ~~a~~ front surface and the ~~a~~ back surface of a substrate. A combined~~composite~~ inductance L11 illustrated ~~shown~~ between the emitter of the lower--arm switching element T2 of the inverter circuit 3 and the lower--arm--driving reference power-supply terminal COM of the high-withstand-voltage ~~compression~~ IC 10 indicates the combined~~composite~~ inductance in a circuit part including the lower--arm diode D2 through which circulating current flows. The combined~~composite~~ inductance L11 can be~~is~~ suppressed to a value between about several~~between a few~~ nH (nano Henri) to about several~~few~~ dozens of nH by taking the aforementioned measures.

[0023] The circulating current flows only for a short period of time, that is, the variation in ~~and an amount of change of~~ current ~~(di/dt)~~ per unit time (di/dt) is large. Therefore~~,~~ ~~and therefore~~, even if the combined~~composite~~ inductance of the circuit part where

circulating current flows is made small, an induced voltage of about several volts is ~~a few voltages of some inductive voltages are~~ generated anyway in that part.~~,~~ The polarity of the induced~~inductive~~ voltage becomes ~~is a~~ negative in which, with respect to the ~~voltage. Specifically, when the~~ potential of the lower-arm-driving reference power-supply terminal COM as a ~~is the~~ reference, the potential of the upper-arm-driving reference power-supply terminal VS becomes ~~is~~ negative. The voltage breakdown of the high-withstand-voltage IC occurs due to this negative voltage.~~Accordingly, compression destruction occurs in the high compression IC.~~ Moreover, this ~~the~~ negative voltage causes the latch-up phenomenon, that is, the phenomenon in which~~-up, i.e.,~~ the driver circuit of the high-withstand-voltage ~~compression~~ IC 10 outputs an erroneous signal.

[0024] In the~~The~~ inverter device according to the first embodiment~~, shown in Fig. 1 includes~~ a clamp diode D10 is provided as a clamping means. Specifically, ~~for clamping a difference in potential between~~ the ~~lower arm driving reference supply terminal COM and the upper arm driving high-pressure side power supply terminal VB to a predetermined voltage. An~~ anode of the clamp diode D10 is connected to the lower-arm-driving reference power-supply terminal COM~~,~~ and the ~~a~~ cathode ~~of the clamp diode D10~~ is connected to the upper-arm-driving high-voltage power-supply terminal VB. This clamp diode D10 clamps a potential difference between the lower-arm-driving reference power-supply terminal COM and the upper-arm-driving high-voltage~~pressure side~~ power-supply terminal VB. The position at which the clamp diode D10 according to the present invention is connected ~~is connected in the~~ is different from the positions of the clamp diodes disclosed in above-mentioned Patent Documents 1 and~~,~~ 2.~~, the reason of which will be described below.~~

[0025] The reason why the clamp diode D10 is connected between the lower-arm-driving reference power-supply terminal COM and the upper-arm-driving high-voltage~~pressure side~~ power-supply terminal VB ~~as shown in Fig. 1,~~ is described with reference to Figs. 2 and 3. Fig. 2 is a diagram~~schematic~~ for explaining why~~describing~~ malfunction of a high-withstand-voltage~~compression~~ IC occurs in an inverter device that does not include ~~in which~~ a clamping means. ~~clamp diode is not connected, and~~ Fig. 3 is a diagram illustrating~~schematic for describing~~ a state in which through current that is to flow into~~flowing toward~~ a high-withstand-voltage~~compression~~ IC is made to flow

into~~drawn to a side of~~ the clamp diode in the inverter device according to the first embodiment.

[0026] In Fig. 2, the internal structure of the high-withstand-voltage IC 10 represented in Fig. 1 is illustrated in more detail. The high-withstand-voltage~~Fig. 2 is a detailed schematic of an inside of the high compression IC 10 shown in Fig. 1. In Fig. 2, the high compression~~ IC 10 includes an input buffer 14, an N~~-channel metal oxide (~~MOS~~)~~ transistor 16, a parasitic diode 17, a resistor 20, and a driver circuit 12. The ~~An~~ input terminal of the input buffer 14 is connected to the upper--arm control--signal input terminal HIN, and the ~~an~~ output terminal is connected to the ~~of the input buffer 14 is connected to a~~ gate of the NMOS transistor 16. The parasitic diode 17 is connected to the NMOS transistor 16 in parallel. The collector~~A corrector~~ of the NMOS transistor 16 is connected to the ~~an~~ input terminal of the driver circuit 12. Moreover, the collector of the NMOS transistor 16 is also~~, and~~ connected to the upper--arm--driving high-voltage~~pressure side~~ power--supply terminal VB via ~~through~~ the resistor 20 whose one end ~~that~~ is connected to the input terminal of the driver circuit 12.

[0027] The~~A~~ mechanism by which~~of a malfunction of~~ the high-withstand-voltage ~~compression~~ IC 10 causes malfunction is described. When~~ next. In Fig. 2, when~~ the upper--arm switching element T1 is turned on, a main circuit current I1, as shown with a dashed ~~indicated by a wavy~~ line, flows in a load 8 that has an inductance component. Subsequently, when~~When~~ the upper--arm switching element T1 is turned off, the current that was flowing through ~~in~~ the load 8 starts flowing into~~flows through~~ the lower--arm diode D2 as a circulating current I2. The circulating current I2 has a steep gradient ~~having an acute inclination and into the load 8~~. As described above, because parts of~~components in~~ the inverter circuit 3 are connected by patterns or ~~and~~ wires, although very small, inductance components exist in these parts.~~and a slight inductor component is present between the components.~~ Among these inductance components, ~~a position of~~ an inductance component in the region where the circulating current I2 flows is denoted by the combined inductance L11 in the figure. An induced~~. Assuming that an inductive~~ voltage VL that is generated in the combined inductance ~~component~~ L11 due to flow of~~when~~ the circulating current I2~~I2 flows through, the inductive voltage VL~~ can be expressed by the following Equation (1).~~equality.~~

[0028]

$VL=L11\times(di/dt)$ (1)

[0029] The lower~~As~~ the impedance of the load 8 is, the steeper the gradient~~decreases, inclination~~ of the circulating~~a~~ current I2 (that is, larger the ration di/dt in Equation (1))~~flow~~ becomes. In other words, the lower the impedance of the load 8 is, the higher the induced~~ more acute (specifically, di/dt in the equality (1) increases), so that the inductive~~ voltage VL is.~~increases.~~

[0030] Furthermore, an on voltage VF is generated across~~in~~ the lower-arm diode D2 when the circulating current I2 flows. As~~Thus,~~ a result, a potential difference expressed by the following Equation (2) ~~in potential~~ occurs between the emitter of the upper-arm switching element T1 and the emitter of the lower-arm switching element T2.~~, as expressed by the following equality:~~

[0031]

$\Delta V=VL+VF$ (2)

[0032] The emitter of the upper-arm switching element T1 and the emitter of the lower-arm switching element T2 are connected to the upper-arm-driving reference power-supply terminal VS and the lower-arm-driving reference power-supply terminal COM ~~of the high compression IC 10~~, respectively. Therefore, a voltage ΔV expressed by Equation~~the equality~~ (2) is applied across ~~between~~ these terminals.

[0033] When the voltage ΔV is applied across the upper-arm-driving reference power-supply terminal VS and the lower-arm-driving reference power-supply terminal COM of the high-withstand-voltage IC 10, a through current I3 flows from the parasitic diode 17 through the resistor 20. This through current I3 is the main cause of the latch-up phenomenon in which the driver circuit 12 outputs an erroneous signal.

~~[0033] The high compression IC 10 includes the input buffer 14, the NMOS transistor 16, the parasitic diode 17, the resistor 20, and the driver circuit 12, and therefore, when ΔV1 is applied, a through current I3 flows from the parasitic diode 17 through the resistor 20. The through current I3 mainly causes the driver circuit 12 to output an erroneous signal, called the latch up phenomenon.~~

[0034] In the~~The~~ inverter device according to the first embodiment, however, as shown in Fig. 3, ~~includes~~ the clamp diode D10 is provided between the lower-arm-driving reference power-supply terminal COM and the upper-arm-driving high-voltage~~pressure side~~ power-supply terminal VB. Because of this clamp diode D10~~, and~~

~~therefore~~, the through current I3, which would flow through the high-withstand-voltage ~~flowing inside the high compression~~ IC 10 in the circuit configuration represented~~shown~~ in Fig. 2, is made to flow into the clamp diode D10. A portion of the through current I3 may flow through the high-withstand-voltage IC 10. However, a substantially large portion of the through current I3 is drawn to the clamp diode D10. The reason is that, the impedance of the ~~2 can be drawn to the clamp diode D10 side as shown in Fig. 3. Part of the through current might flow in the high compression IC 10, however, an impedance in the~~ clamp diode D10 connected between the same terminals, i.e., the terminals COM and VB, ~~terminal~~ is smaller than an impedance of the ~~in a~~ series circuit configured with ~~of~~ a parasitic diode D17 and the resistor 20 through which the through current I3 flows in~~. Therefore, a large portion of the through current I3 can be drawn to the clamp diode D10 side, so that the through current I3 that flows inside~~ the high-withstand-voltage IC 10. Accordingly, the through current I3 that flows through the high-withstand-voltage~~-compression~~ IC 10 can be reduced substantially, and malfunction of the high-withstand-voltage IC 10 caused due to the ~~by~~ latch--up phenomenon can be prevented from occurring.~~.~~

[0035] In the inverter devices ~~device~~ disclosed in Patent Documents 1 and 2, on the other hand, the ~~patent documents 1, 2, one terminal (~~cathode~~)~~ of the clamp diode is connected to the upper--arm--driving reference power-supply terminal VS. Therefore~~Thus~~, the effect of drawing~~conventional clamp diode cannot draw~~ the through current in the configuration disclosed in Patent Documents 1 and 2 is smaller than that in the case of~~as much as~~ the clamp diode D10 of the first embodiment.

[0036] In the ~~The~~ inverter device according to the first embodiment, the cathode of the clamp diode D10 is connected to the upper--arm--driving high-voltage~~pressure side~~ power--supply terminal VB (for example, -+15V terminal) of the high-withstand-voltage IC 10. Therefore, ~~compression IC 10, and therefore,~~ the current flowing through the clamp diode D10 can be reduced compared to the current flowing through the clamp diode, for example, disclosed in Patent Documents 1 and~~,~~ 2. Hence~~Therefore~~, a diode of a smaller current rating compared to the clamp diode disclosed in Patent Documents 1 and 2 can be selected for the clamp diode D10.~~, 2 can be employed in the first embodiment.~~

[0037] As described above, in the inverter device according to the first embodiment, the

clamp diode D10 is provided~~connected~~ between the lower-~~-~~arm-~~-~~driving reference power-supply terminal COM ~~of the high compression IC~~ and the upper-~~-~~arm-~~-~~driving high-voltage~~pressure side~~ power-~~-~~supply terminal VB of the high-withstand-voltage ~~compression~~ IC 10. The clamp diode D10 clamps a potential difference ~~in potential~~ between the lower-~~-~~arm-~~-~~driving reference power-supply terminal COM and the upper-arm-~~-~~driving high-voltage~~pressure side~~ power-~~-~~supply terminal VB. As a result, breakdown~~. Therefore, destruction~~ and malfunction of the high-withstand-voltage ~~compression~~ IC 10 can be ~~is~~ prevented without increasing the ~~, and increases in~~ circuit scale or ~~and~~ cost.~~ is suppressed.~~

[0038] In the first embodiment, the clamp diode D10 is shown ~~is attached on the~~ outside of the high-withstand-voltage ~~compression~~ IC; however,~~, but~~ the clamp diode D10 can be provided ~~attached on the~~ inside of the high-withstand-voltage ~~compression~~ IC. However, it is advantageous to provide~~attach~~ the clamp diode ~~on the~~ outside of the high-withstand-voltage ~~compression~~ IC;~~,~~ because, in that case it is not necessary to change the design of the high-withstand-voltage ~~compression~~ IC, i.e., the first embodiment ~~and the present invention~~ can be applied to an inverter device employing an existing high-withstand-voltage ~~compression~~ IC.

[0039] Furthermore, in the first embodiment, a diode is used as the clamping means;~~ for clamping a difference in potential between the lower arm driving reference supply terminal and the upper arm driving high-pressure side power supply terminal,~~ however, the clamping means is not limited to a~~the~~ diode. Any element that turns on at a voltage higher than a certain value and that can output an approximately ~~voltage and outputs a substantially~~ constant voltage can be used~~, such~~ as the clamping means. As the clamping means, for example, a PN junction of a Zener~~zener~~ diode or a PN junction of a bipolar transistor can be used.~~,~~

[0040] Second Embodiment

Fig. 4 is a schematic for explaining an inverter device according to a second embodiment of the present invention. The inverter device according to the first embodiment is ~~included~~ a single-phase inverter circuit, whereas the inverter device according to the second embodiment is ~~includes~~ a three-phase inverter circuit. In other words, the~~The~~ inverter device of the second embodiment includes ~~shown in Fig. 4 employs a configuration of a typical~~ three pairs of switching elements. Specifically,

the ~~-phase~~ inverter device of the second embodiment includes ~~, in which~~ an inverter driving unit 2a and an inverter circuit 3a. The inverter circuit 3a includes three upper-arm ~~including a high compression IC 10a drives upper arm~~ switching elements T1, T3, T5 and three lower--arm switching elements T2, T4, T6. The driving unit 2a, which includes a high-withstand-voltage IC 10a, drives the six switching elements of the ~~an~~ inverter circuit 3a. The structural elements ~~The inverter device according to the second embodiment is described with reference to Fig. 4. The components~~ in the second embodiment that are~~perform~~ same or equivalent to ~~similar function or that have same or similar configuration as~~ those in the first embodiment will be ~~are~~ denoted by the same reference numerals as in the first embodiment, and overlapping descriptions are simplified or omitted.

[0041] The inverter circuit 3a ~~shown in Fig. 4~~ includes a bridge circuit 6a and the DC power supply 7. The bridge circuit 6a includes three upper arm units 4a, 4b, 4c, and three lower arm units 5a, 5b, 5a. The ~~an~~ upper arm unit 4a includes~~including~~ the upper--arm switching element T1 and the upper--arm diode D1 connected in reverse-parallel~~back-to-back~~ to each other. The~~, an~~ upper arm unit 4b includes~~including~~ the upper--arm switching element T3 and an upper--arm diode D3 connected in reverse-parallel~~back-to-back~~ to each other. The~~, an~~ upper arm unit 4c includes~~including~~ the upper--arm switching element T5 and an upper--arm diode D5 connected in reverse-parallel~~back-to-back~~ to each other. The~~, a~~ lower arm unit 5a includes~~including~~ the lower--arm switching element T2 and a lower--arm diode D2 connected in reverse-parallel~~back-to-back~~ to each other. The~~, a~~ lower arm unit 5b includes~~including~~ the lower--arm switching element T4 and a lower--arm diode D4 connected in reverse-parallel~~back-to-back~~ to each other. The ~~, and a~~ lower arm unit 5c includes~~including~~ the lower--arm switching element T6 and a lower--arm diode D6 connected in reverse-parallel~~back-to-back~~ to each other. A bridge circuit 6a is configured by series connecting the upper arm unit 4a to the lower arm unit 5a, the upper arm unit 4b to the lower arm unit 5b, and the upper arm unit 4c to the lower arm unit 5c. The ~~Each of the back-to-back connection circuits, the upper arm units 4a, 4b, 4c, are connected in series to each of the back-to-back connection circuits, the lower arm units 5a, respectively, in a bridge circuit 6a. In the bridge circuit 6a, the~~ positive electrode of the DC power supply 7 is connected to the collectors~~each corrector~~ of the

upper-~~-~~arm switching elements T1, T3, T5, and the negative electrode ~~of the DC power supply 7~~ is connected to the emitters~~each emitter~~ of the lower-~~-~~arm switching elements T2, T4, T6.~~ Thus, the inverter circuit 3a shown in Fig. 4 has a configuration of a three-phase inverter circuit.~~

[0042] The high-withstand-voltage~~-compression~~ IC 10a ~~in the inverter driving unit 2a shown in Fig. 4~~ drives the upper-~~-~~arm switching elements T1, T3, T5, and the lower-~~-~~arm switching elements T2, T4, T6.~~, in the inverter circuit 3a.~~ The high-withstand-voltage~~-compression~~ IC 10a has various ~~includes~~ input/output terminals described below. Specifically, the ~~terminals are the~~ high-withstand-voltage IC 10a has the terminal VDD that is a high-voltage~~pressure side~~ power-~~-~~supply terminal;~~, for control VDD,~~ the terminal COM that is a reference power-supply terminal;~~for control COM,~~ the upper-~~-~~arm control-~~-~~signal input terminal HIN;~~,~~ the lower-~~-~~arm control-~~-~~signal input terminal LIN, upper-~~-~~arm-~~-~~driving high-voltage~~pressure side~~ power-~~-~~supply terminals VB1, VB3, VB5;~~,~~ upper-~~-~~arm-~~-~~driving reference power-supply terminals VS1, VS3, VS5;~~,~~ upper-~~-~~arm switching-~~-~~element driving-~~-~~signal output terminals HO1, HO3, HO5;~~,~~ the lower-~~-~~arm-~~-~~driving high-voltage~~pressure side~~ power-~~-~~supply terminal VCC;~~,~~ the lower-~~-~~arm-~~-~~driving reference power-supply terminal COM;~~,~~ and lower-~~-~~arm switching-element driving-~~-~~signal output terminals LO2, LO4, LO6.

[0043] The~~Decoupling condensers C1, C3, C5 are connected between each terminal of the~~ upper-~~-~~arm-~~-~~driving high-voltage~~pressure side~~ power-~~-~~supply terminals VB1, VB3, VB5 are connected to~~and each terminal of~~ the upper-~~-~~arm-~~-~~driving reference power-supply terminals VS1, VS3, VS5 via ~~, respectively. The~~ decoupling capacitors C1, C3, C5, respectively. Moreover,~~condenser C2 is connected between~~ the lower-~~-~~arm-~~-~~driving high-voltage~~pressure side~~ power-~~-~~supply terminal VCC is connected to ~~and~~ the lower-arm-~~-~~driving reference power-supply terminal COM via a decoupling capacitor C2.

[0044] The upper-arm switching-element driving-signal output terminal HO1 is connected to the upper-arm switching element T1 via a gate resistor R1. The upper-arm switching-element driving-signal output terminal HO3 is connected to the upper-arm switching element T3 via a gate resistor R3. The upper-arm switching-element driving-signal output terminal HO5 is connected to the upper-arm switching element T5 via a gate resistor R5. Moreover, the upper-arm-driving reference power-supply terminal VS1 is directly connected to the emitter of the upper-arm switching element T1, the

upper-arm-driving reference power-supply terminal VS3 is directly connected to the emitter of the upper-arm switching element T3, and the upper-arm-driving reference power-supply terminal VS5 is directly connected to the emitter of the upper-arm switching element T5. Furthermore, the lower-arm switching-element driving-signal output terminals LO2 is connected to the gate of the lower-arm switching element T2 via a gate resistor R2. The lower-arm switching-element driving-signal output terminals LO4 is connected to the gate of the lower-arm switching element T4 via a gate resistor R4. The lower-arm switching-element driving-signal output terminals LO6 is connected to the gate of the lower-arm switching element T6 via a gate resistor R6. Moreover, the lower-arm-driving reference power-supply terminal COM is directly connected to the emitters of the lower-arm switching elements T2, T4, T6.

[0045] The lower-arm-driving reference power-supply terminal COM is connected to the upper-arm-driving high-voltage power-supply terminals VB1, VB3, VB5 via clamp diodes D11, D12, D13, respectively. Specifically, the anodes of the clamp diodes D11, D12, D13 are connected to the lower-arm-driving reference power-supply terminal COM. Thus, in the inverter device according to the second embodiment, the clamp diodes D11, D12, D13 function as a clamping unit that clamps a potential difference between the lower-arm-driving reference power-supply terminal COM and each of the upper-arm-driving high-voltage power-supply terminals VB1, VB3, VB5 to a certain voltage.~~,~~

~~[0044] In between the inverter circuit 3a and the high compression IC 10a, each terminal of the upper arm switching element driving signal output terminals HO1, HO3, HO5 and each gate of the upper arm switching elements T1, T3, T5 are connected by gate resistors R1, R3, R5, respectively. Each terminal of the upper arm driving reference supply terminals VS1, VS3, VS5 is directly connected to each emitter of the upper arm switching elements T1, respectively. Similarly, each terminal of the lower arm switching element driving signal output terminals LO1, HO3, HO5 and each gate of the lower arm switching elements T2, T4, T6 are connected by gate resistors R2, R4, R6, respectively. The lower arm driving reference supply terminal COM is directly connected to each emitter of the lower arm switching elements T2.~~

~~[0045] The inverter device according to the second embodiment includes clamp diodes D11, D12, D13 as clamping arrangement for clamping a difference in potential between~~

~~the lower arm driving reference supply terminal COM and each terminal of the upper arm driving high-pressure side power supply terminals VB1, VB3, VB5 to a predetermined voltage. Each anode of the clamp diodes D11, D12, D13 is connected to the lower arm driving reference supply terminal COM, and each cathode of the clamp diodes D11, D12, D13 is connected to each terminal of the upper arm driving high-pressure side power supply terminals VB1, VB3, VB5, respectively.~~

~~[0046] Thus, in the inverter device according to the second embodiment, similarly to the first embodiment, a large portion of through current flowing toward the inside of the high compression IC 10a can be drawn to the side of the clamp diodes D11, D12, D13, so that the through current that flows toward the high compression IC 10 can be reduced, and malfunction caused by latch up can be prevented.~~

~~[0047] Furthermore, in the inverter device according to the second embodiment, each cathode of the clamp diodes D11, D12, D13 is connected to each terminal of the upper arm driving high-pressure side power supply terminals VB1, VB3, VB5, respectively. Therefore, current flowing through the clamp diodes D11, D12, D13 can be reduced compared to current flowing through the clamp diode disclosed in Patent Documents 1, 2. Accordingly, a diode of a smaller current rating compared to the clamp diode disclosed in Patent Documents 1, 2 can be employed in the second embodiment.~~

~~[0048] As described above, the inverter device according to the second embodiment, each clamp diode connected between each terminal of the lower arm driving reference supply terminal of the high compression IC and each terminal of the upper arm driving high-pressure side power supply terminal of the high compression IC, respectively, clamps each difference in potential between the lower arm driving reference supply terminal and each terminal of the upper arm driving high-pressure side power supply terminal. Therefore, destruction and malfunction of the high compression IC is prevented, and increases in circuit scale and cost is suppressed.~~

~~[0049] In the second embodiment, each clamp diode is attached on the outside of the high compression IC, but the clamp diode can be attached on the inside of the high compression IC. However, it is advantageous to attach the clamp diode on the outside of the high compression IC, because it is not necessary to change the design of the high compression IC, and the present invention can be applied to an inverter device employing an existing high compression IC.~~

~~[0050] Furthermore, in the second embodiment, a diode is used as the clamping arrangement for clamping each difference in potential between the lower arm driving reference supply terminal and each terminal of the upper arm driving high-pressure side power supply terminal, however, the clamping arrangement is not limited to the diode. Any element that turns on at a certain voltage and outputs a substantially constant voltage can be used, such as a zener diode or a PN junction of a bipolar transistor.~~

~~[0051]Third Embodiment~~

[0046] Thus, in the inverter device according to the second embodiment, in the same manner as the first embodiment, a substantial portion of the through current that would normally flow into the high-withstand-voltage IC 10a can be drawn to the clamp diodes D11, D12, D13. Accordingly, the through current that flows into the high-withstand-voltage IC 10a can be reduced, and malfunction due to the latch-up phenomenon can be prevented from occurring.

[0047] In the inverter device according to the second embodiment, cathodes of the clamp diodes D11, D12, D13 are connected to the upper-arm-driving high-voltage power-supply terminals VB1, VB3, VB5, respectively. Therefore, the current flowing through the clamp diodes D11, D12, D13 can be reduced compared to the ~~Fig. 5 is a schematic for explaining an inverter device according to a third embodiment of the present invention. The inverter device according to the second embodiment includes independent power supplies for individually driving each switching element in the upper arm unit, and a common power supply for driving each switching element in the lower arm unit, whereas in the inverter device according to the third embodiment, each switching element in the upper and lower arm units are driven by a common power supply. Therefore, a connection configuration of the clamp diodes is different from that of the second embodiment. The components in the third embodiment that perform same or similar function or that have same or similar configuration as those in the second embodiment are denoted by the same reference numerals as in the first embodiment, and overlapping descriptions are omitted.~~

~~[0052] The inverter device according to the third embodiment shown in Fig. 5 includes a first clamp diode D10 and second clamp diodes D21, D22, D23 as clamping arrangement for clamping a difference in potential between the lower arm driving reference supply terminal COM and each terminal of the upper arm driving high-~~

~~pressure side power supply terminals VB1, VB3, VB5 to a predetermined voltage. An anode of the first clamp diode D10 is connected to the lower arm driving reference supply terminal COM, and a cathode of the first clamp diode D10 is connected to the lower arm driving high-pressure side power supply terminal VCC. Each anode of the second clamp diodes D21, D22, D23 is connected to the lower arm driving high-pressure side power supply terminal VCC, and each cathode of the second clamp diodes D21, D22, D23 is connected to each terminal of the upper arm driving high-pressure side power supply terminals VB1, VB3, VB5, respectively.~~

~~[0053] Thus, in the inverter device according to the third embodiment, similarly to the inverter devices according to the first and second embodiments, a large portion of through current flowing toward the inside of the high compression IC 10a can be drawn to the side of the first clamp diode D10 and the second clamp diodes D11, D12, D13, so that the through current that flows toward the inside the high compression IC 10 can be reduced, and malfunction caused by latch up can be prevented.~~

~~[0054] Furthermore, in the inverter device according to the third embodiment, each cathode of the second clamp diodes D21, D22, D23 is connected to each terminal of the upper arm driving high-pressure side power supply terminals VB1, VB3, VB5, respectively. Therefore, current flowing through the second clamp diodes D21, D22, D23 can be reduced compared to~~ current flowing through the clamp diode, for example, disclosed in Patent Documents 1 and ~~,~~2. Hence~~Therefore~~, a diode of a smaller current rating compared to the clamp diode disclosed in Patent Documents 1 and ~~,~~2 can be selected for the clamp diodes D11, D12, D13.

[0048~~employed in the third embodiment.~~

~~[0055~~] As described above, in the inverter device according to the second ~~third~~ embodiment, the ~~first~~ clamp diodes D11, D12, D13 are connected between the lower-arm-~~-~~driving reference power-supply terminal COM and each of the upper-~~of the high compression IC and the lower~~ arm-~~-~~driving high-voltage~~pressure side~~ power-~~-~~supply terminal VB1, VB2, VB3 of the high-withstand-voltage IC 10a. Each of the diodes D11, D12, D13 clamps potential differences~~compression IC, and the second clamp diodes connected~~ between the lower-~~-~~arm-~~-~~driving reference~~high-pressure side~~ power-~~-~~supply terminal COM~~of the high compression IC~~ and ~~each terminal of~~ the upper-~~-~~arm-~~-~~driving high-voltage~~pressure side~~ power-~~-~~supply terminals VB1, VB2, VB3.~~of the high~~

~~compression IC clamp each difference in potential between the lower arm driving reference supply terminal and each terminal of the upper arm driving high-pressure side power supply terminals.~~ Therefore, breakdown~~destruction~~ and malfunction of the high-withstand-voltage IC 10a can be ~~compression IC is~~ prevented without increasing the~~,~~ ~~and increases in~~ circuit scale or~~and~~ cost.

[0049~~is suppressed.~~

~~[0056~~] In the second~~third~~ embodiment, ~~each clamp diode is attached on~~ the clamp diodes D11, D12, D13 are shown outside of the high-withstand-voltage~~compression~~ IC 10a; however,~~, but~~ the clamp diode diodes D11, D12, D13 can be provided ~~attached on the~~ inside of the high-withstand-voltage~~compression~~ IC 10a.~~.~~ However, it is advantageous to provide~~attach~~ the clamp diodes D11, D12, D13~~diode on the~~ outside of the high-withstand-voltage IC 10a;~~compression IC,~~ because, in that case it is not necessary to change the design of the high-withstand-voltage IC, i.e., the second embodiment~~compression IC, and the present invention~~ can be applied to an inverter device employing an existing high-withstand-voltage IC.

[0050~~compression IC.~~

~~[0057~~] Furthermore, in the second~~third~~ embodiment, a diode is used as the clamping means; however, the clamping means is not limited to a diode. Any element that turns on at a voltage higher than a certain value and that can output an approximately constant voltage can be used as the clamping means. As the clamping means, for example, a PN junction of a Zener diode or a PN junction of a bipolar transistor can be used.

[0051] Third Embodiment

Fig. 5 is a schematic for explaining an inverter device according to a third embodiment of the present invention. The inverter device according to the second embodiment employs individual power supplies for individually driving the switching elements of the upper arm units, and employs a common power supply for commonly driving the switching elements of the lower arm units. On the other hand, the inverter device according to the third embodiment employs a common power supply for driving the switching element of both the upper and lower arm units. Therefore, a connection configuration of the clamp diodes in the inverter device according to the third embodiment is different from that in the second embodiment. The other components are same or equivalent to those in the second embodiment and they have been denoted

by the same reference numerals as in the second embodiment, and their description has been omitted.

[0052] The inverter device according to the third embodiment includes, as a clamping means, a first clamp diode D10 and three second clamp diodes D21, D22, D23. The anode of the first clamp diode D10 is connected to the lower-arm-driving reference power-supply terminal COM, and the cathode is connected to the lower-arm-driving high-voltage power-supply terminal VCC. The anodes of the second clamp diodes D21, D22, D23 are connected to the lower-arm-driving high-voltage power-supply terminal VCC, and the cathodes are connected to the upper-arm-driving high-voltage power-supply terminals VB1, VB3, VB5, respectively. The clamping means clamps the potential differences between the lower-arm-driving reference power-supply terminal COM and each of the upper-arm-driving high-voltage power-supply terminals VB1, VB3, VB5 to a certain voltage.

[0053] Thus, in the inverter device according to the third embodiment, in the same manner as the first and second embodiments, a substantial portion of the through current that would normally flow into the high-withstand-voltage IC 10a can be drawn to the first clamp diode D10 and the second clamp diodes D21, D22, D23. Accordingly, the through current that flows into the high-withstand-voltage IC 10a can be reduced, and malfunction due to the latch-up phenomenon can be prevented from occurring.

[0054] In the inverter device according to the third embodiment, the cathodes of the second clamp diodes D21, D22, D23 are connected to the upper-arm-driving high-voltage power-supply terminals VB1, VB3, VB5, respectively. Therefore, the current flowing through the second clamp diodes D21, D22, D23 can be reduced compared to the current flowing through the clamp diode disclosed, for example, in Patent Documents 1 and 2. Hence, a diode of a smaller current rating compared to the clamp diode disclosed in Patent Documents 1 and 2 can be selected~~arrangement~~ for the clamp diodes D21, D22, D23.

[0055] As described above,~~clamping each difference~~ in the inverter device according to the third embodiment, the first clamp diode D10 is connected~~potential~~ between the lower-arm-driving reference power-supply terminal COM and ~~each terminal of~~ the lower-~~upper~~-arm-driving high-voltage power-supply terminal VCC of the high-withstand-voltage IC 10a, and the second clamp diodes D21, D22, D23 are connected

between the lower-arm-~~-~~driving high-voltage power-supply terminal COM and the upper-arm-driving high-voltage power-supply terminals VB1, VB3, VB5, respectively. The second clamp diodes D21, D22, D23 clamp potential differences between the lower-arm-driving reference power-supply terminal COM and the upper-arm-driving high-voltage power-~~pressure side power~~ supply terminals VB1, VB2, VB3, respectively. Therefore, breakdown and malfunction of the high-withstand-voltage IC 10a can be prevented without increasing the circuit scale or cost.

[0056] In the third embodiment, the clamp diodes D10, D21, D22, D23 are shown outside of the high-withstand-voltage IC 10a; however, the clamp diode diodes D10, D21, D22, D23 can be provided inside of the high-withstand-voltage IC 10a. However, it is advantageous to provide the clamp diodes D10, D21, D22, D23 outside of the high-withstand-voltage IC 10a; because, in that case it is not necessary to change the design of the high-withstand-voltage IC, i.e., the third embodiment can be applied to an inverter device employing an existing high-withstand-voltage IC.

[0057] Furthermore, in the third embodiment, a diode is used as the clamping means;~~,~~ however, the clamping means~~arrangement~~ is not limited to a~~the~~ diode. Any element that turns on at a ~~certain~~ voltage higher than a certain value and that can output an approximately~~outputs a substantially~~ constant voltage can be used~~, such~~ as the clamping means. As the clamping means, for example, a PN junction of a Zener~~zener~~ diode or a PN junction of a bipolar transistor can be used.~~.~~

INDUSTRIAL APPLICABILITY

[0058] As described above, the~~an~~ inverter device according to the present invention can be widely applied to an inverter device including, for example, a single-phase inverter circuit or a three-phase inverter circuit. Moreover, the~~, and is particularly suitable as an~~ inverter device according~~specifically required~~ to the present invention is particularly suitable for an inverter device that requires prevention of~~prevent~~ malfunction and voltage breakdown~~compression destruction~~ of a high-withstand-voltage~~ compression~~ IC.

ABSTRACT

~~In an inverter device, destruction and malfunction (latch up) of a high compression IC is prevented.~~

An inverter device includes an inverter circuit, an inverter driving unit, and a clamp diode. The inverter ~~(3) including a bridge~~ circuit includes ~~(6) connected between a positive electrode and a negative electrode of a direct current power supply (7), the bridge circuit including~~ an upper arm unit ~~(4)~~ and a lower arm unit ~~(5)~~ connected in series. The ~~, wherein the~~ upper arm unit and the lower arm unit include ~~includes a upper arm~~ switching elements that drive a load. The inverter driving unit ~~element (T1) and a diode (D1) connected back-to-back to each other, and the lower arm unit~~ includes a high-withstand-voltage IC that drives the ~~lower arm~~ switching elements of the upper arm unit and the lower arm unit. The~~element (T2) and a diode (D2) connected back-to-back to each other; an inverter driving unit (2) including a~~ high-withstand-voltage ~~compression~~ IC has a first terminal for supplying a reference voltage to~~(10) that drives the upper arm switching element and~~ the lower arm unit and a second terminal for supplying a high-voltage to the upper arm unit. The clamp diode ~~switching element; and a clamp unit (D10) that~~ clamps a potential difference ~~in potential~~ between ~~a lower-arm driving reference supply terminal of the high compression IC and an upper arm driving high-pressure side power supply terminal of~~ the first terminal and the second terminal.~~high compression IC.~~